What is claimed is:

1. A semiconductor package in which multiple chips are embedded,

each chip including a common circuit having substantially the same common function,

the common circuit in a selected one of the chips being enabled,

the common circuit in one or more other ones of the chips being disabled, and

the enabled common circuit performing the common function for the selected chips and the one or more other chips.

2. The semiconductor package of claim 1, wherein at least one of the multiple chips is a semiconductor memory chip.

3. The semiconductor package of claim 1, wherein at least one of the multiple chips is a microprocessor chip.

4. The semiconductor package of claim 1, wherein at least one of the multiple chips is a microprocessor chip, and at least one of the other chips is a memory chip.

5. The semiconductor package of claim 1, wherein multiple chips comprise two chips.

6. The semiconductor package of claim 1, wherein the common circuit includes a power generator.

7. The semiconductor package of claim 1, wherein the common circuit includes a clock buffer.

8. The semiconductor package of claim 1, wherein the common circuit includes a signal generator.

9. A semiconductor package which multiple chips are embedded,

each of the chips including a common circuit having substantially the same common function and a selection circuit,

the common circuit in a selected one of the chips not being disabled via the corresponding selection circuit,

the common circuit in one or more of the other ones of the chips being disabled via the corresponding selection circuit, and

the non-disabled common circuit performing the common function for the selected chip and for the one or more other chips.

10. The semiconductor package of claim 9, wherein at least one of the multiple chips is a semiconductor memory chip.

11. The semiconductor package of claim 9, wherein at least one of the multiple chips is a microprocessor chip.

12. The semiconductor package of claim 9, at least one of the multiple chips is a microprocessor chip, and at least one of the other chips is a semiconductor memory chip.

13. The semiconductor package of claim 9, wherein the multiple chips comprise two chips.

14. The semiconductor package of claim 9, wherein the common circuit includes a power generator.

15. The semiconductor package of claim 9, wherein the common circuit includes a clock buffer.

16. The semiconductor package of claim 9, wherein the common circuit includes a signal generator.

17. A method of reducing current consumption in a semiconductor package in which multiple chips are to be embedded, the method comprising:

providing multiple chips, each chip including a common circuit having substantially the same common function;

enabling the common circuit in a selected one of the chips;

disabling the common circuit in one or more other ones of the chips so as to reduce current otherwise consumed thereby;

coupling the enabled common circuit and the one or more disabled common circuits such that the enabled common circuit performs the common function for the selected chip and the other chips.

18. The method of claim 17, wherein:

each of the chips includes a selection circuit;

the disabling of the common circuit in the one or more other chips includes coupling a disabling voltage to the selection circuit therein, respectively; and

the enabling of the common circuit in the selected chip includes not coupling a voltage to the selection circuit therein.

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